PCB EMC Design Guidelines: A Brief Annotated List

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EMC Design Guideline Collection

Board Level – Trace routing

- No trace unrelated to I/O should be located between an I/O connector and the device(s) sending and receiving signals using that connector.
- All power planes and traces should be routed on the same layer.
- A trace with a propagation delay more than half the transition time of the signal it carries must have a matched termination.
- Capacitively-loaded nets must have a total source impedance equal to or greater than one-quarter of the line characteristic impedance or a series resistor must be added to meet this condition.
- Nets driven at faster than 1V/ns slew rate must have a discrete series resistor at the source.
- Guard traces should be used to isolate high-speed nets from I/O nets.
- Guard traces should be connected to the ground plane with vias located less than one-quarter wavelength apart at the highest frequency of interest.
- All power and ground traces must be at least three times the nominal signal line width. This does not include guard traces.
- If a ground or power separation is required, the gap must be at least 3 mm wide.
- Additional decoupling capacitors should be placed on both sides of a power or ground plane gap.
- Critical nets should be routed in a daisy chain fashion with no stubs or branches.
- Critical nets should be routed at least 2X from the board edge, where X is the distance between the trace and its return current path.
- Signals with high-frequency content should not be routed beneath components used for board I/O.
- Differential pairs radiate much less than single-ended signals even when the traces in the pair are separated by many times their distance above a ground plane. However, imbalance in the pair can result in radiation comparable to an equivalent single-ended signal.
- The length of high-frequency nets should be minimized.
- The number of vias in high-frequency nets should be minimized.
- On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component.
- Gaps or slots in the ground plane should be avoided. They should ONLY be used in situations where it is necessary to control the flow of low-frequency (i.e. less than 100 kHz) currents.

EMC Design Guideline Collection

Board Level – Decoupling (boards with closely spaced power/ground planes)

- *On boards with closely spaced (i.e. less than 0.25 mm) power and ground planes, the location of decoupling capacitors is not nearly as important as the inductance associated with their connection to the planes.*
- *Decoupling capacitors should be connected directly to power/ground planes using vias in or adjacent to the pads.*
- *It is unnecessary and ineffective to use capacitors with a nominal value that is less than the board's interplane capacitance. At low frequencies, higher values of capacitance are desirable. At high frequencies, connection inductance is much more important than the nominal value of the capacitor.*
- *Power supply leads from active devices and decoupling capacitors should be connected directly to the power and ground planes. No attempt should be made to connect chip leads directly to a decoupling capacitor.*

Board Level – Decoupling (boards with widely spaced power/ground planes)

- *On boards with widely spaced (i.e. greater than 0.5 mm) power and ground planes, a local decoupling capacitor should be located near each active device. If the active device is mounted on the side of the board nearest the ground plane, the decoupling capacitor should be located near the power pin. If the active device is mounted on the side of the board nearest the power plane, the decoupling capacitor should be located near the ground pin.*
- *Decoupling capacitors should be connected directly to power/ground planes using vias in or adjacent to the pads. Decoupling capacitors can share a power or ground via with the active device if this can be accomplished without traces (or with a traces length less than the power/ground plane spacing).*
- *Power supply leads from active devices and decoupling capacitors should be connected directly to the power and ground planes. No attempt should be made to connect chip leads directly to a decoupling capacitor. Decoupling capacitors can share a power or ground via with the active device if this can be accomplished without traces (or with a traces length less than the power/ground plane spacing).*
- *It is unnecessary and ineffective to use capacitors with a nominal value that is less than the board's interplane capacitance. At low frequencies, higher values of capacitance are desirable. At high frequencies, connection inductance is much more important than the nominal value of the capacitor.*

Board Level – Decoupling (boards with no power plane)

- *On boards with no power plane, a local decoupling capacitor should be located near each active device. The inductance of the decoupling capacitor connection between power and ground should be minimized. Two local decoupling capacitors with a few centimeters of space between them, can be used to provide more effective decoupling than a single capacitor.*

EMC Design Guideline Collection

Board Level – Component Placement

- Connectors should be located on one edge or on one corner of a board.
- No high-speed circuitry should be located between I/O connectors.
- Generally, a board with a solid ground plane will perform better than a board without one.
- Critical signal traces should be buried between power/ground planes.
- Active digital components should be selected that have maximum acceptable off-chip transition times.
- A device on the board that communicates with a device off the board through a connector should be located as close as possible (e.g. within 2 cm) to that connector.
- All off-board communication from a single device should be routed through the same connector.
- Components not connected to an I/O net should be located at least 2 cm away from I/O nets and connectors.
- Clock drivers should be located adjacent to clock oscillators.

Board Level – General

- On boards with multiple signal return planes, all vias connected to one signal return plane should also connect to the others.

EE371 Design Problem

UNIVERSITY OF MISSOURI-ROLLA
ELECTROMAGNETIC COMPATIBILITY LABORATORY

Printed Circuit Board Layout Guidelines

1. Keep loop areas small (signal paths, decoupling) (minimize inductance, radiation).
2. Place components before routing traces.
3. Locate components to minimize length of high frequency and I/O lines.
4. Route ground first, then power, then I/O traces, then high-speed traces, then slower traces.
5. Connectors are the best interface to possible antennas! Don't allow high speed signals to flow between connectors. Place all I/O on one edge of the board if possible.
6. Avoid letting I/O come too far on to the board and keep I/O away from high frequency lines.
7. Leave space for a filter or choke on I/O lines during layout.
8. Unused logic gate inputs should be tied to ground or Vcc.
9. Spacing between any trace and the board edge should be greater than the height of the trace above its return plane.
10. Traces on adjacent layers should be at right angles to each other.
11. Do not permit floating areas of metal.
12. Fill empty areas of the board with metal grounded to the return plane.
13. If possible, the highest speed traces should be sandwiched between planes.
14. Do not allow pigtail connections of ground to connector shell. Use low inductance connections.
15. Lateral separation is more effective than vertical separation.
16. Choose logic families that are no faster than necessary.

Power and Ground Distribution

1. Provide low inductance power and ground to every active component.
2. Layout the ground first, then power, then I/O, then the high frequency lines, then the rest.
3. Divide circuit board into different DC power voltage areas.
4. Do not allow different DC voltage planes to overlap one another.
5. Gaps can be used for kHz currents, but when the ground plane is gapped, all planes should be gapped in the same place.
6. Traces must not cross a gap in the ground plane.
7. The board should have ONE well-defined ground at or near the connectors (don't split).
8. Watch out for via holes cutting slots in the ground plane.
9. Provide at least one decoupling capacitor for each I.C.
10. Provide bulk decoupling where power comes on to the board (~10X the sum of all other decoupling caps).
11. Minimize the series inductance of any lumped decoupling capacitors.

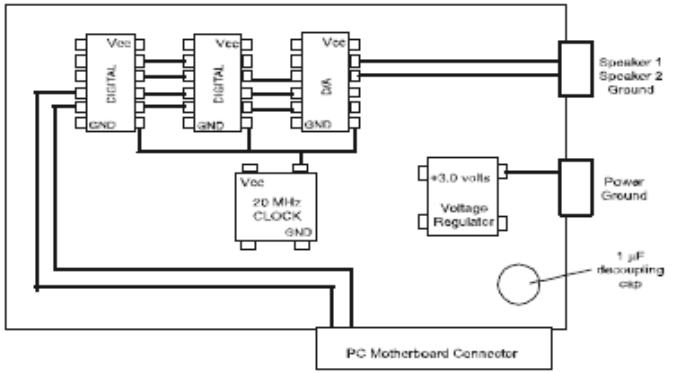
Connector Pin Assignments

1. Layout the board first, then assign connector pins.
2. Provide plenty of ground pins (all connected directly to the return plane).
3. Separate high level and low level signal pins. Use power or return pins to help provide isolation.
4. Any extra pins should be connected to ground.

EE371 Homework #9 **due 11/11/03**

Problem 1: (50 points) A simplified design for a personal computer sound card is shown below. The board has 4 layers with the components on top. The traces shown are on layer 1. Layer 2 is a solid +3.3-volt power plane. Layer 3 is a solid ground plane. Layers 2 and 3 are spaced 40 mils (1 mm) apart. Layer 4 is empty. The board is powered by the motherboard. The board is capable of supplying +3.0-volt power to external speakers through a separate connector.

This device fails to meet the radiated emissions requirements. Show how you would layout the board to reduce radiated emissions. Don't forget to add decoupling capacitors.



Printed Circuit Board Layout Guidelines

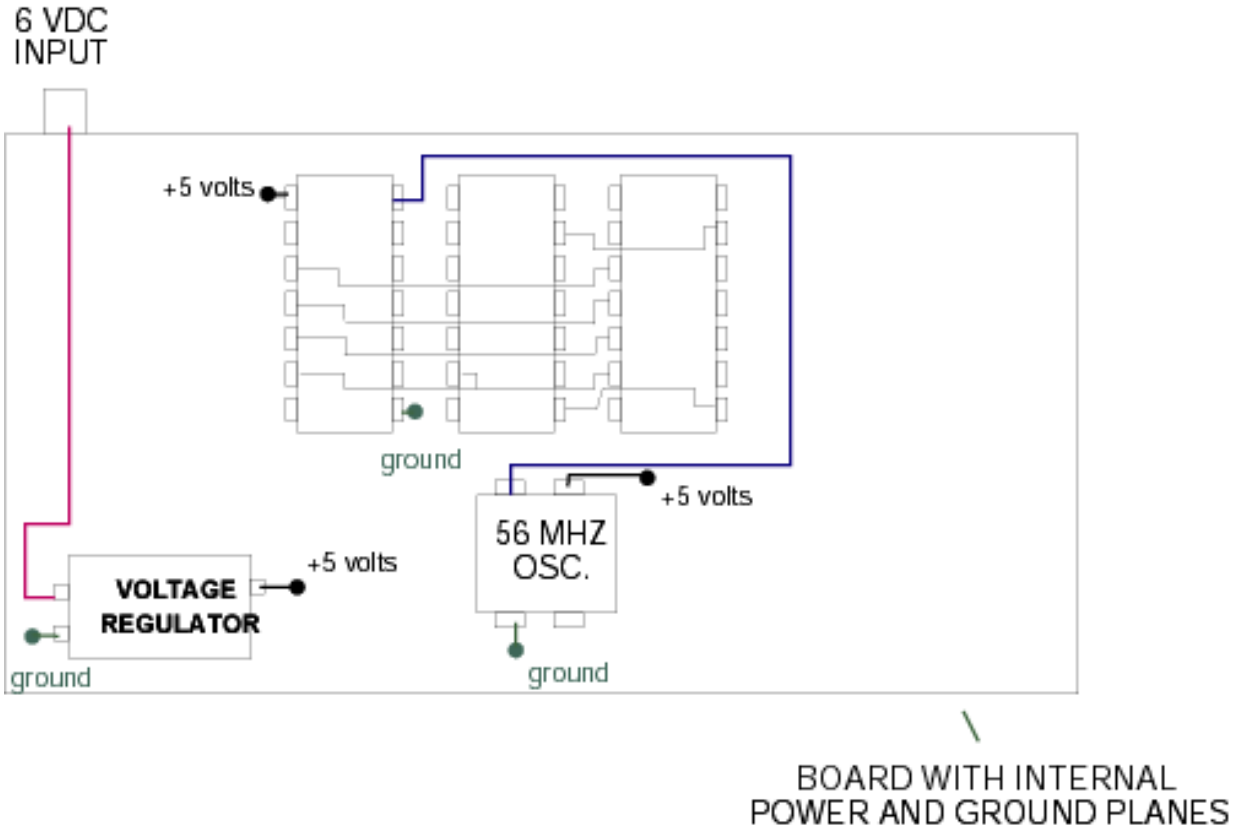
Just tell me what rules I need to follow to ensure that I don't have EMC-related problems with my printed circuit board design.

Printed Circuit Board Layout Guidelines

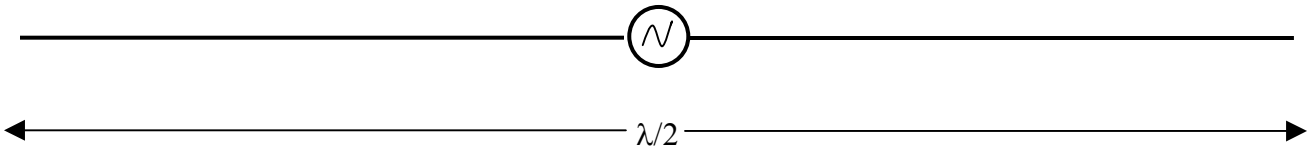
Just tell me what rules I need to follow to ensure that I don't have health-related problems with my brain surgery.

Visualize Return Currents

Where does the 56 MHz return current flow?

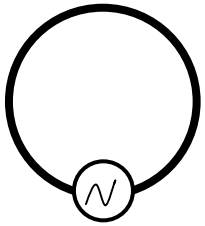


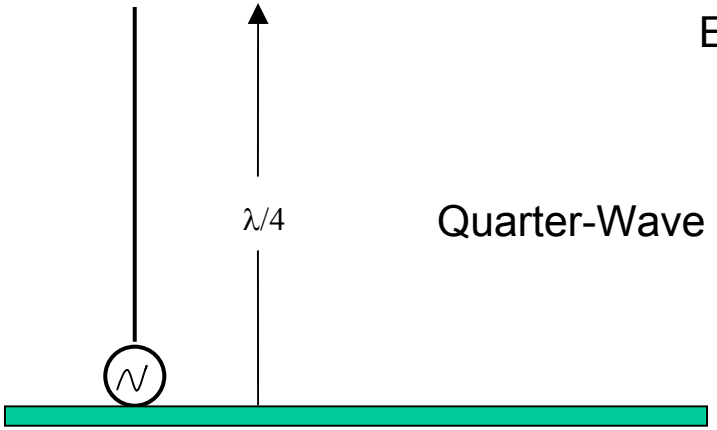
What makes an efficient antenna?



Half-Wave Dipole

Electrically Small Loop

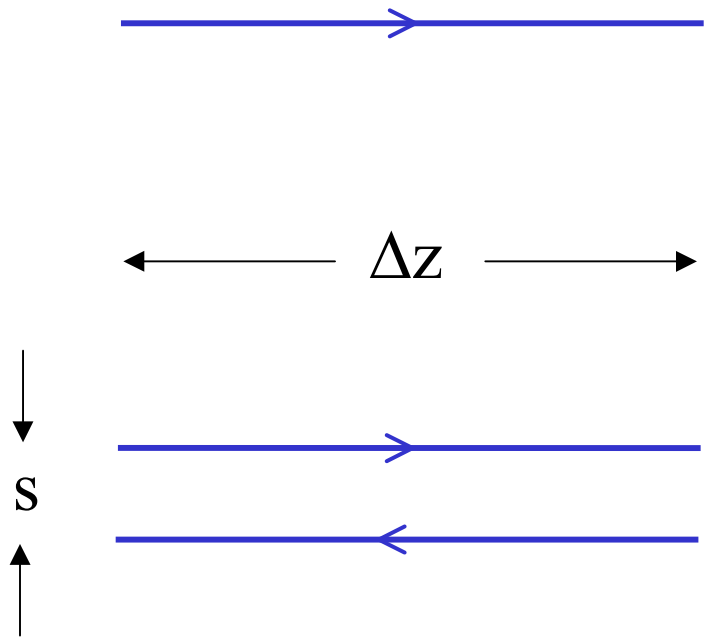




Quarter-Wave Monopole

- **Size**
- **Two Halves**

Common-Mode vs. Differential Mode



$$E_{max} = 1.26 \times 10^{-6} \frac{|I_c| f \Delta z}{r}$$

$$E_{max} = 1.32 \times 10^{-14} \frac{|I_d| f^2 s \Delta z}{r}$$

$$= 4 \times 10^{-6} \frac{|I_d| f \Delta z}{r} \left(\frac{s}{\lambda} \right)$$

Printed Circuit Board Layout Guidelines

Design rules won't make you a good circuit board designer:

- Use common sense!
- Visualize signal current paths
- Locate antennas and crosstalk paths
- Be aware of potential EMI sources

Design Guideline Review

Most important guidelines:

- Keep signal loop areas small
- Don’t locate circuitry between connectors
- Control transition times in digital signals
- Never cut gaps in a solid return plane

Keep signal loop areas small

Why?

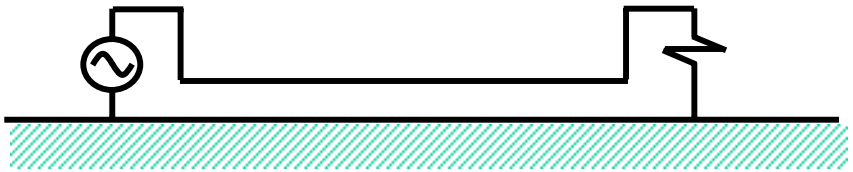
- Radiation from circuits?

Keep signal loop areas small

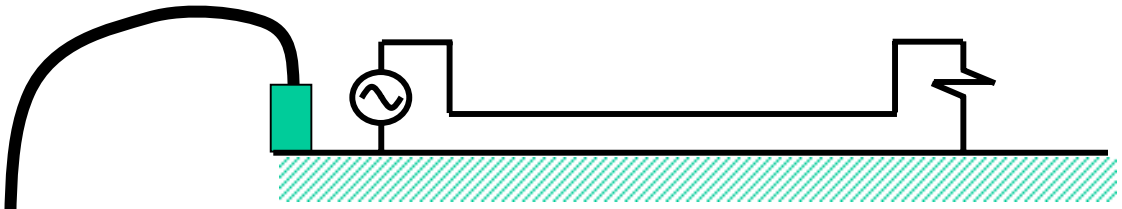
Why?

- Radiation from circuits
- Circuit inductance
- Coupling from circuit

Keep signal loop areas small

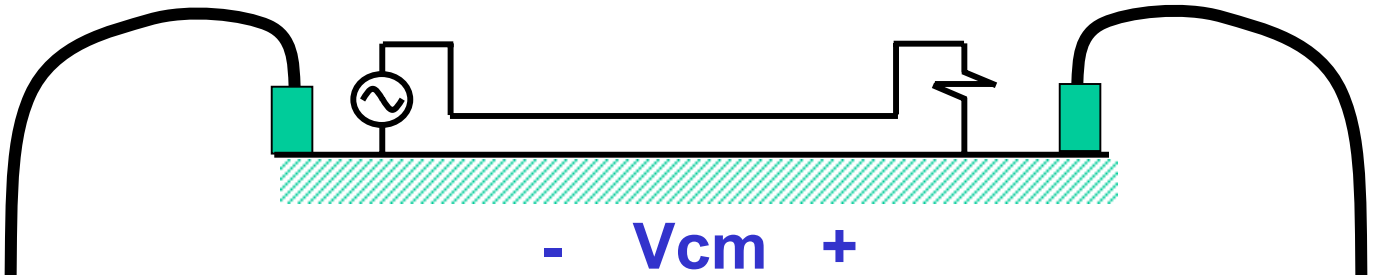


Keep signal loop areas small

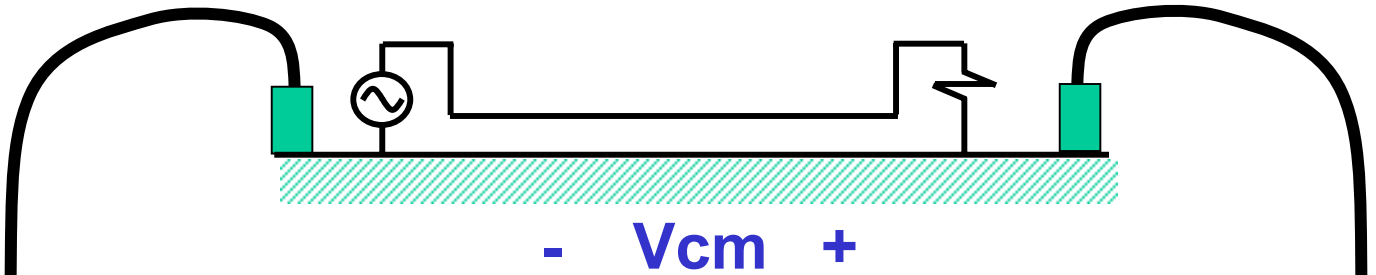


CURRENT DRIVEN

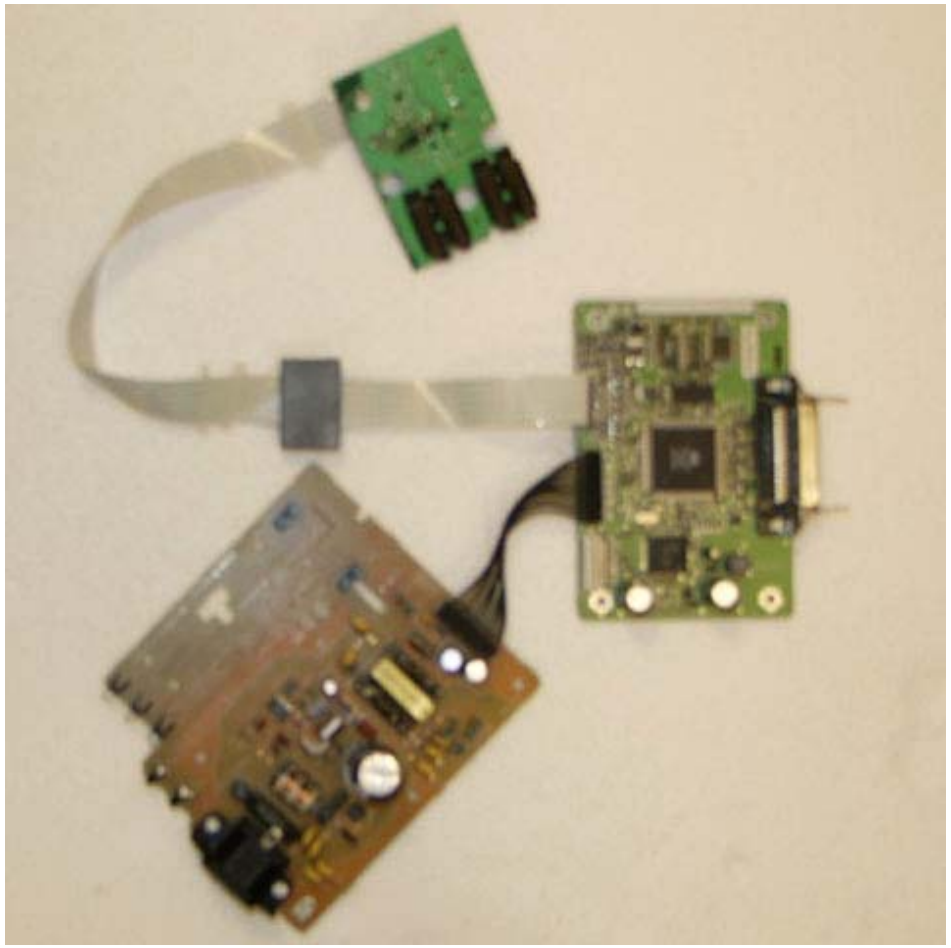
Keep signal loop areas small



Don’t locate HS circuitry between connectors!



Don’t locate HS circuitry between connectors!

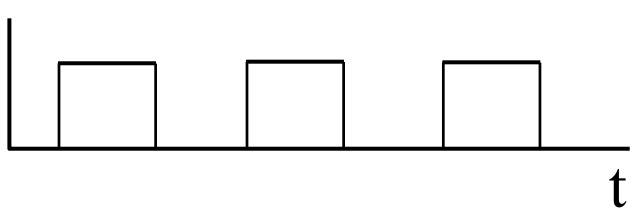


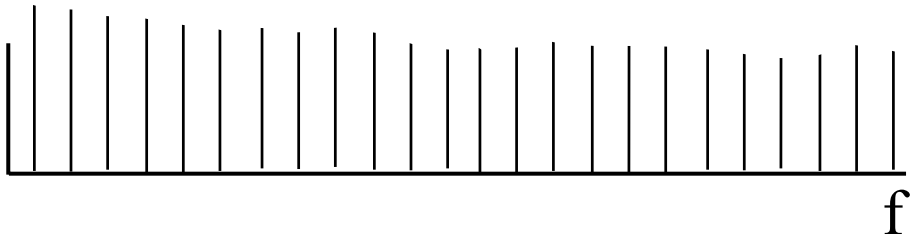
Provide a good HF chassis gnd at connector

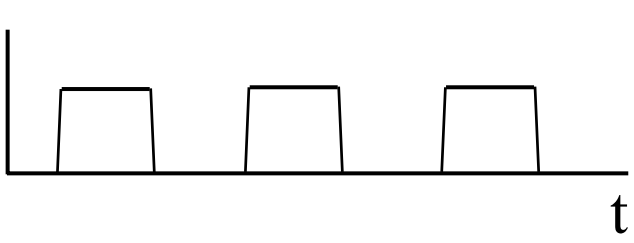
Exceptions

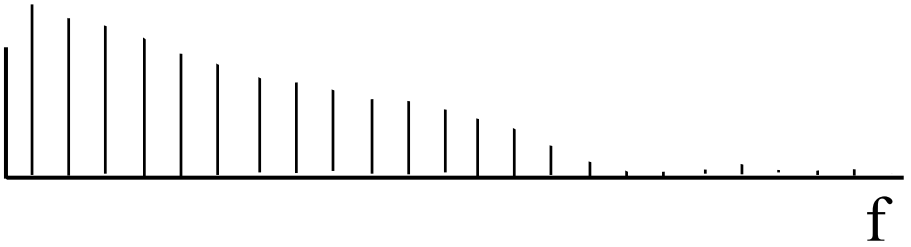
- When there is no chassis ground
- When there are no connectors with cables

Control transition times in digital signals!





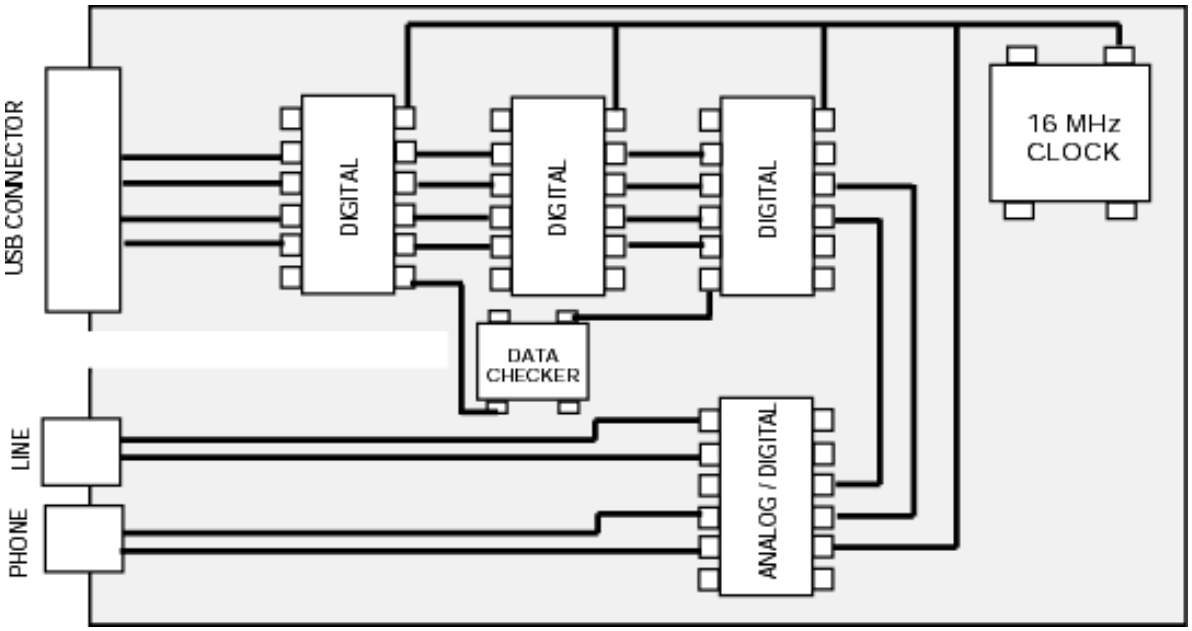




Can use a series resistor or ferrite when load is capacitive.

Use appropriate logic for fast signals with matched loads.

(Almost) Never gap a solid ground plane



(Almost) Never gap a solid ground plane

Why?

- Enhances potential differences in ground
- Makes routing difficult
- Usually creates more problems than it solves

(Almost) Never gap a solid ground plane

Exceptions

- When necessary to prevent common-impedance coupling at frequencies below 100 kHz.
- ?
- ?

Other good design guidelines

Provide adequate decoupling

Boards with no planes

- Bulk decoupling where power comes onto the board.
- Local decoupling near every active device

Provide adequate decoupling

Boards with power and gnd planes > 0.5 mm apart:

- Bulk decoupling where power comes onto the board.
- Local decoupling near every active device

Provide adequate decoupling

Boards with power and gnd planes < 0.25 mm apart:

- Bulk decoupling anywhere.
- Local decoupling spread around the board

Additional design guidelines

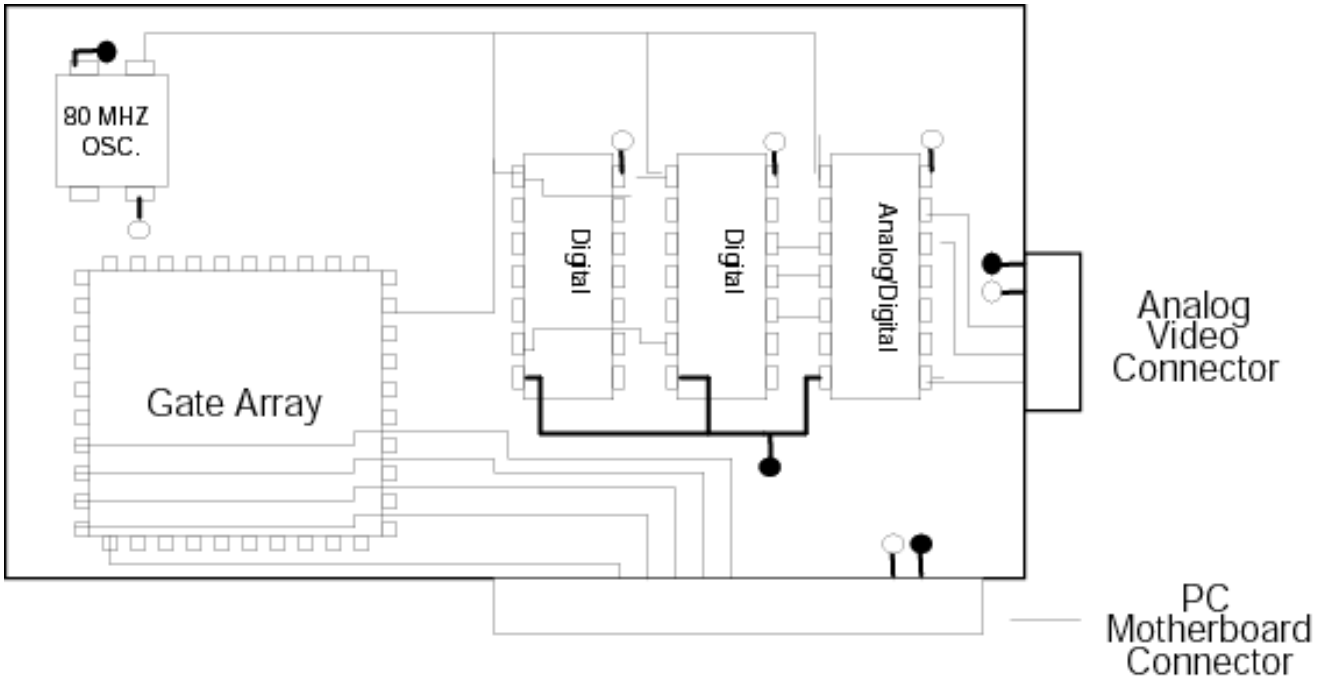
- Keep I/O lines short
- Never gap between connectors
- Keep clock lines short
- Route highest frequencies on inner layers

Other design rules you may have heard of,

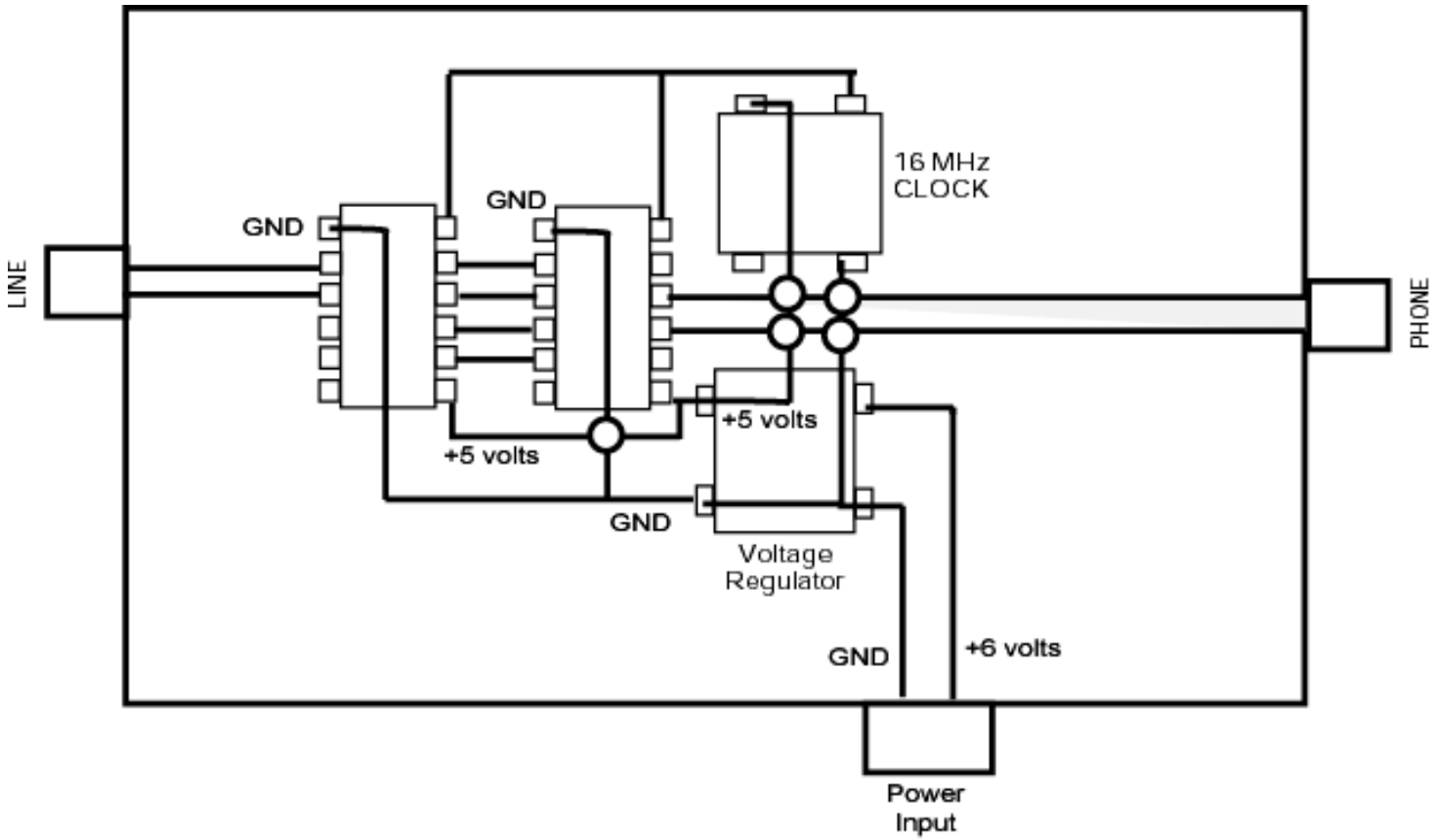
but shouldn't be too concerned with:

- Avoid right angle corners on traces.
- 20-H rule
- Multiple decoupling cap values or traces on caps
- Maximum trace lengths on striplines or microstrips

Design Examples



Design Examples



Summary

Design rules won't make you a good circuit board designer:

- Use common sense!
- Visualize signal current paths
- Locate antennas and crosstalk paths
- Be aware of potential EMI sources
- Seek design advice when you need it